

# Analysis and Design of Phase-Locked Loops by Using CppSim and Matlab

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## **Abstract**

*This paper presents the implementation of a phase-locked loop (PLL), with detailed analysis of several design options. For the simulation of the PLL, a GUI-based tool for the transfer function level PLL design was provided within the package. The theoretical phase noise and jitter performance was calculated. Using this tool and the CppSim programs several frequency synthesizers were implemented.*